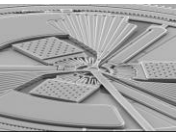
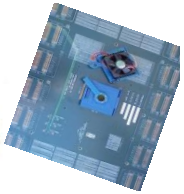
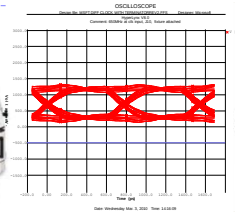
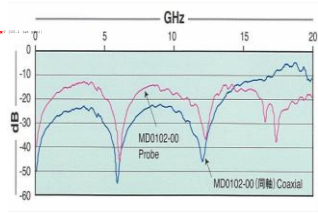




Bridging the Structural & Functional Gap

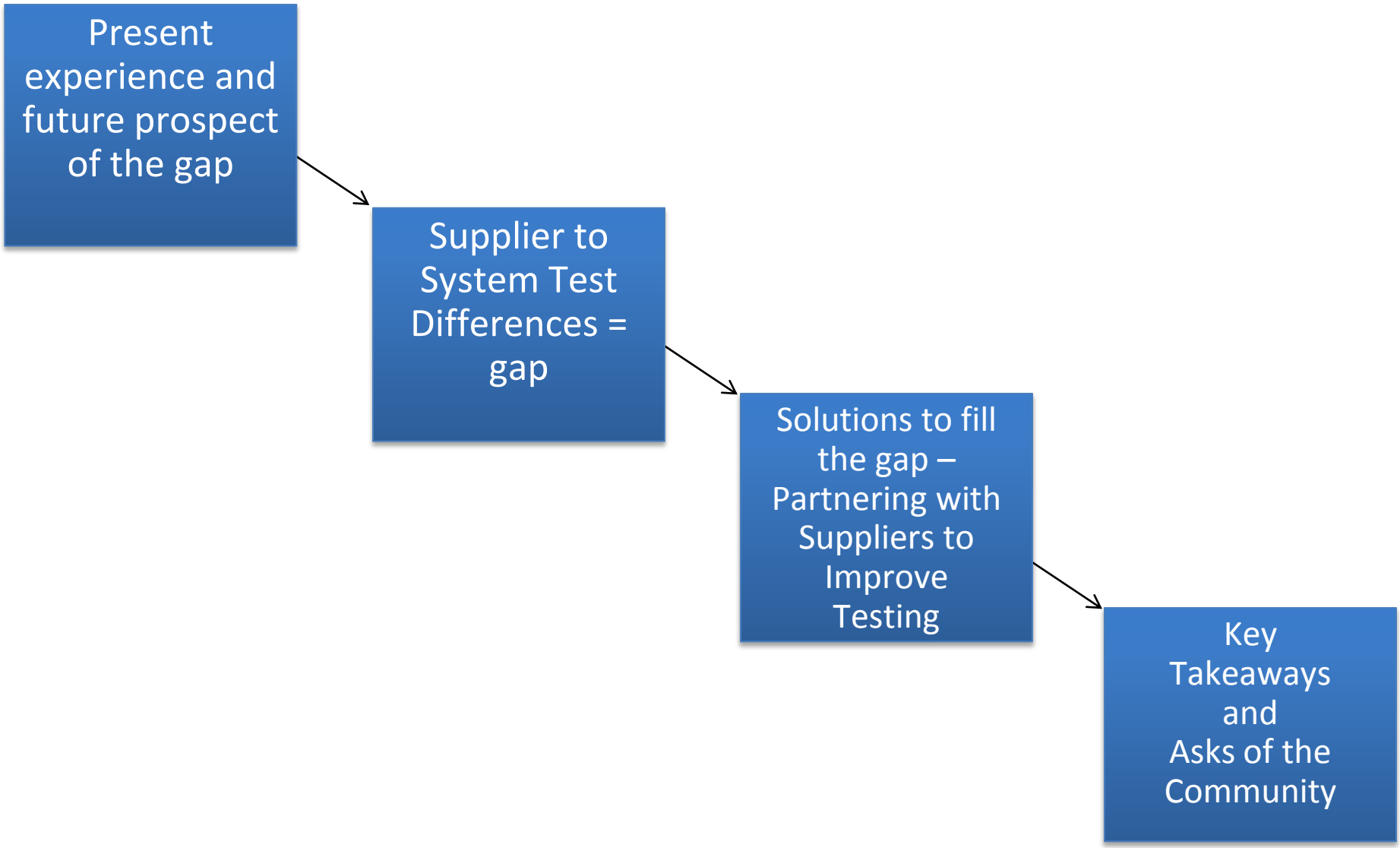
Douglas Kay, Cisco, dkay@cisco.com

Acknowledgements & Clarification

The work presented here has been the effort and collaboration of many people over the last couple of years:

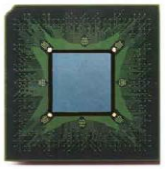
- Cisco
  - Central Test Group
  - Product Operations
  - Engineering ASIC Development
  - DFT Group
  - ASIC Suppliers
- Title of presentation
  - Bridging the gap between standalone component level and embedded system level tests

Outline of presentation



What is your experience?

ASIC
Standalone
Test @ vendor
ATE



Board / system
Test @ MFG
& Field

Stringent Vendor Test Screening

No fail @ MFG process and field?

Our experience: continued high DPPM and field returns

Supplier standalone component tests

Board / System tests (normal and corner condition)

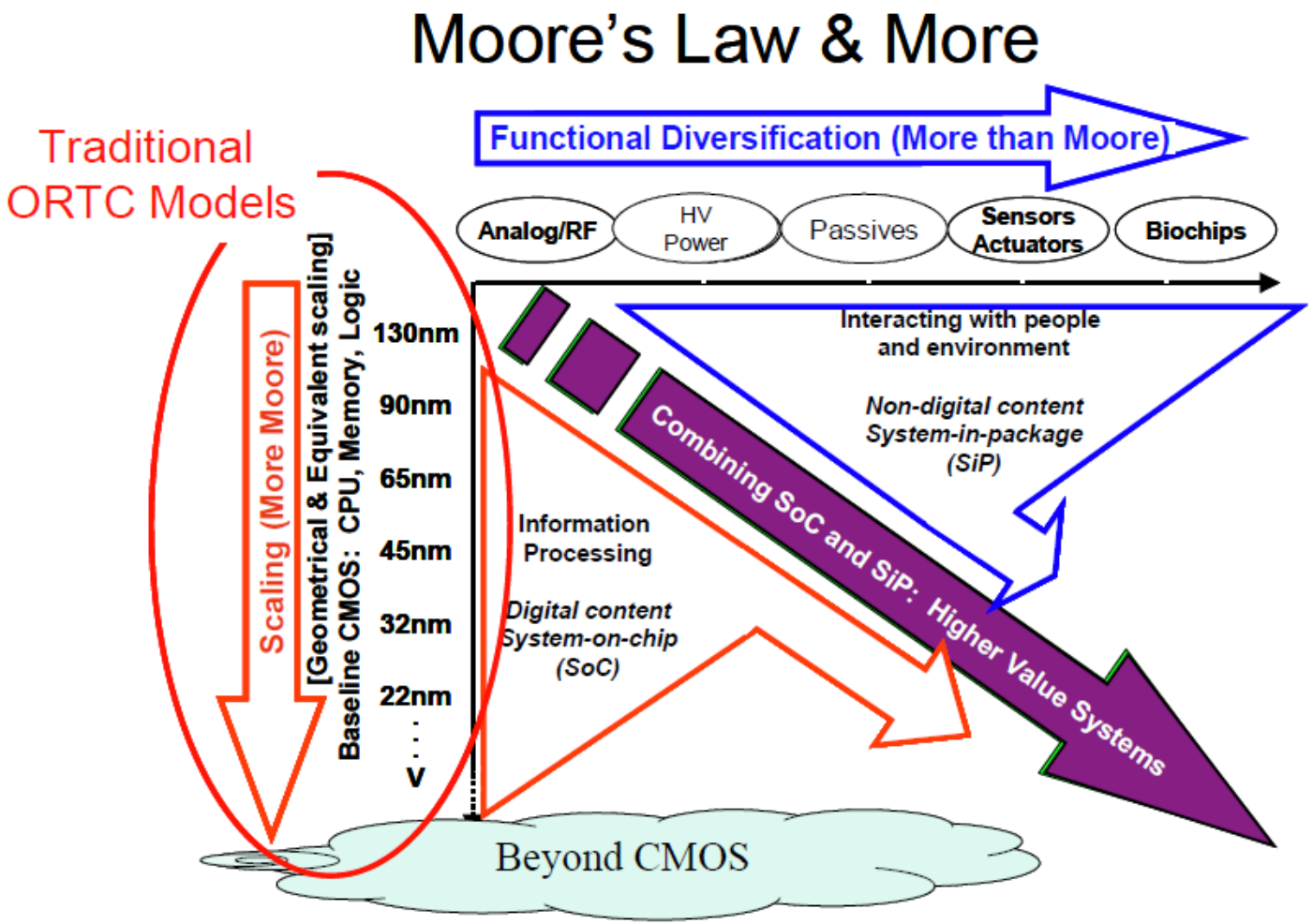
All ASICs meet or exceed DFT and supplier test requirements.

So why do we still have board yields not meeting goal, FCS (First Customer Shipment) delays, field returns?

The size of impact by the gap

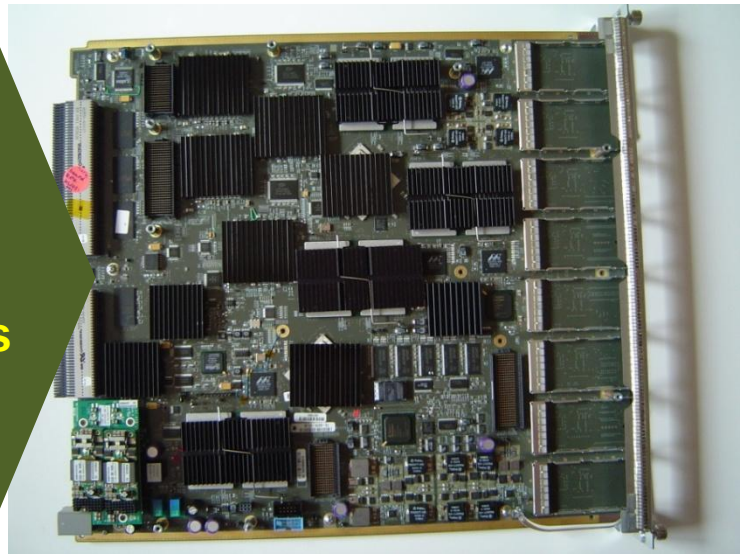
- Cost Penalty:
  - High ASIC replacement and FA costs
    - Average $70K / month (Hard dollar)
  - Unrealized Sale Revenue
    - Case by case (Soft dollar)
    - Usually impacts are more severe than what we realize
- Schedule Penalty:
  - Time to resolve FA
  - Average 18 months to closed ATE test gap
- Average Total cost per ASIC
  - Total = (Average cost per month) X (18 months)
  - Total = ($70,000) X (18 months) = 1.26 millions

What is the prospect of this gap?



ATE to System: Environments

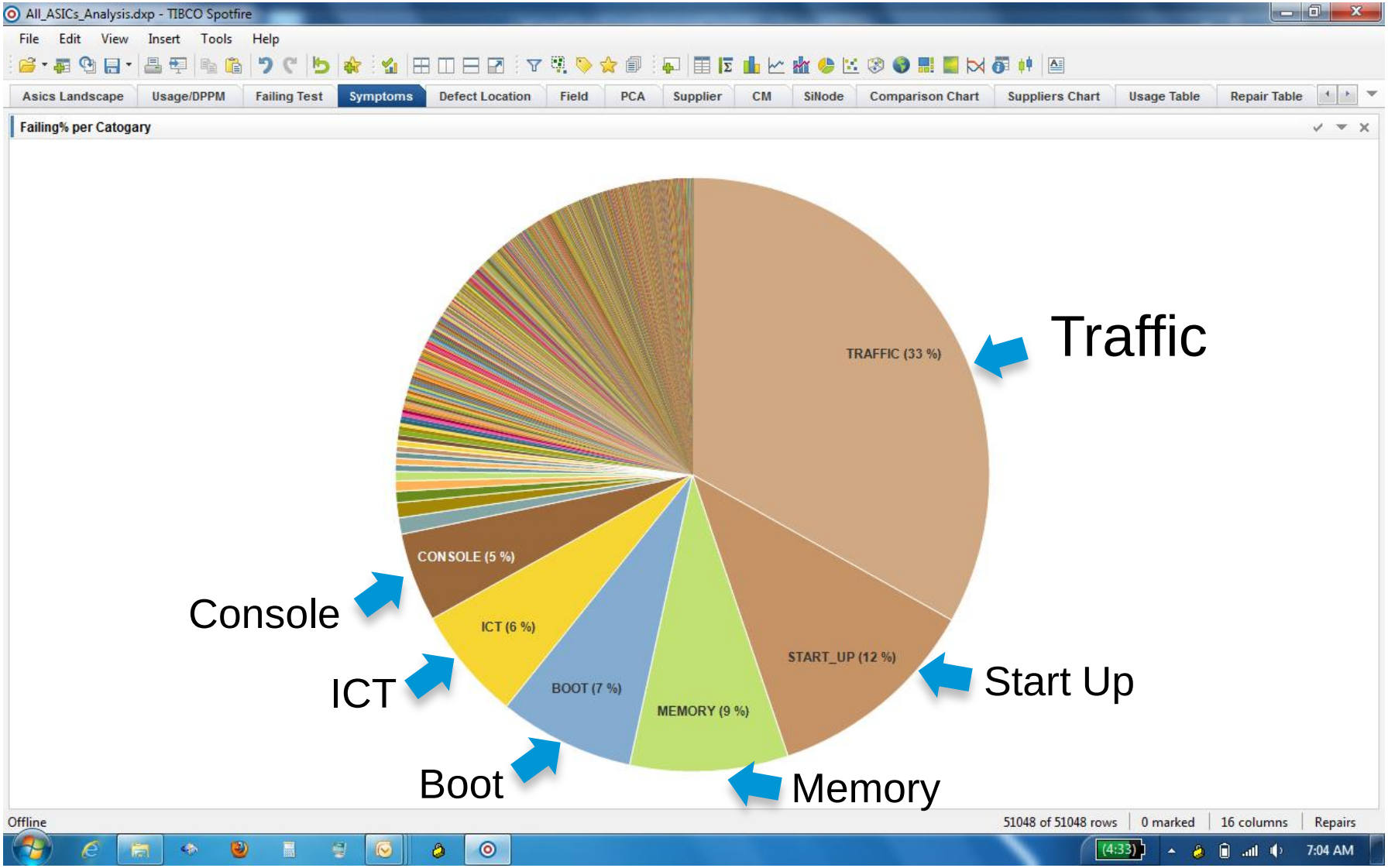
Different test environments and techniques



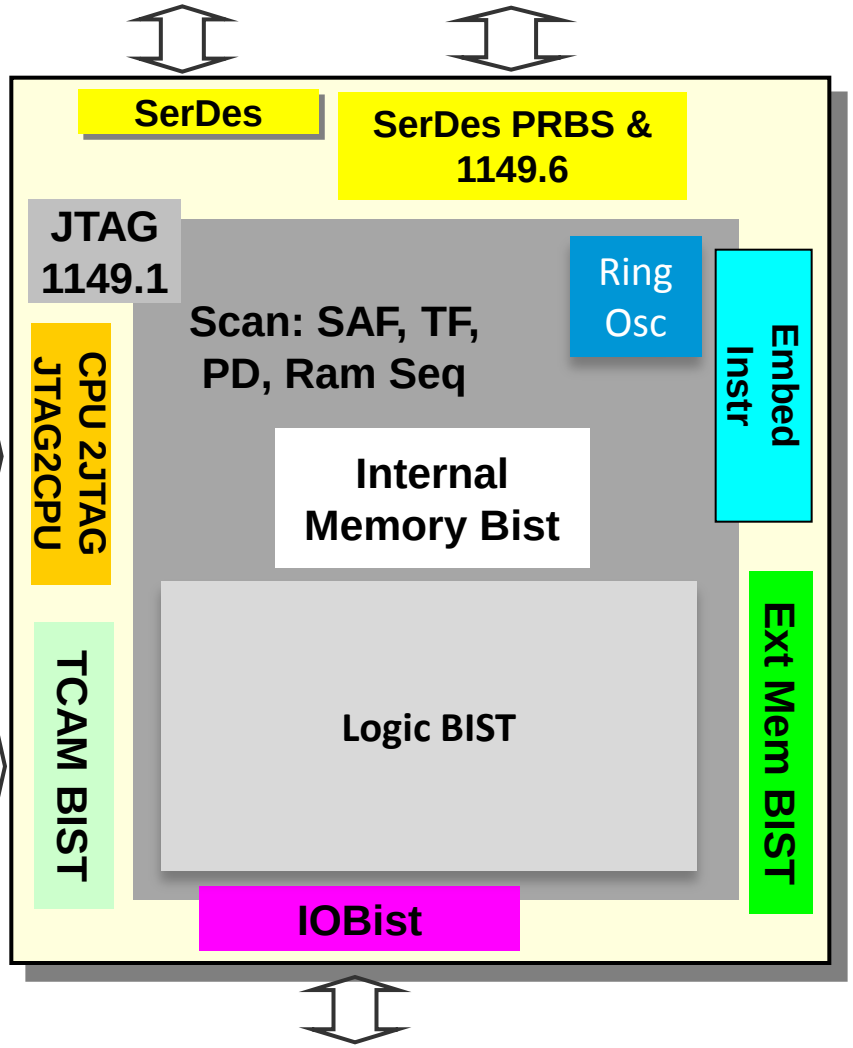
- ‘Structural’ scan and BIST tests
- Low noise, 50 ohm test loadboard
- One component, with fast ‘one-shot’ tests at ASIC spec limits
- Stable controlled temperature
- Very accurate power supplies

- Traffic functional test
- Complex system board design
- Multiple chips interfacing to each other, with long test run times
- Minimal temperature control, less accurate power supplies
- Noisy environment

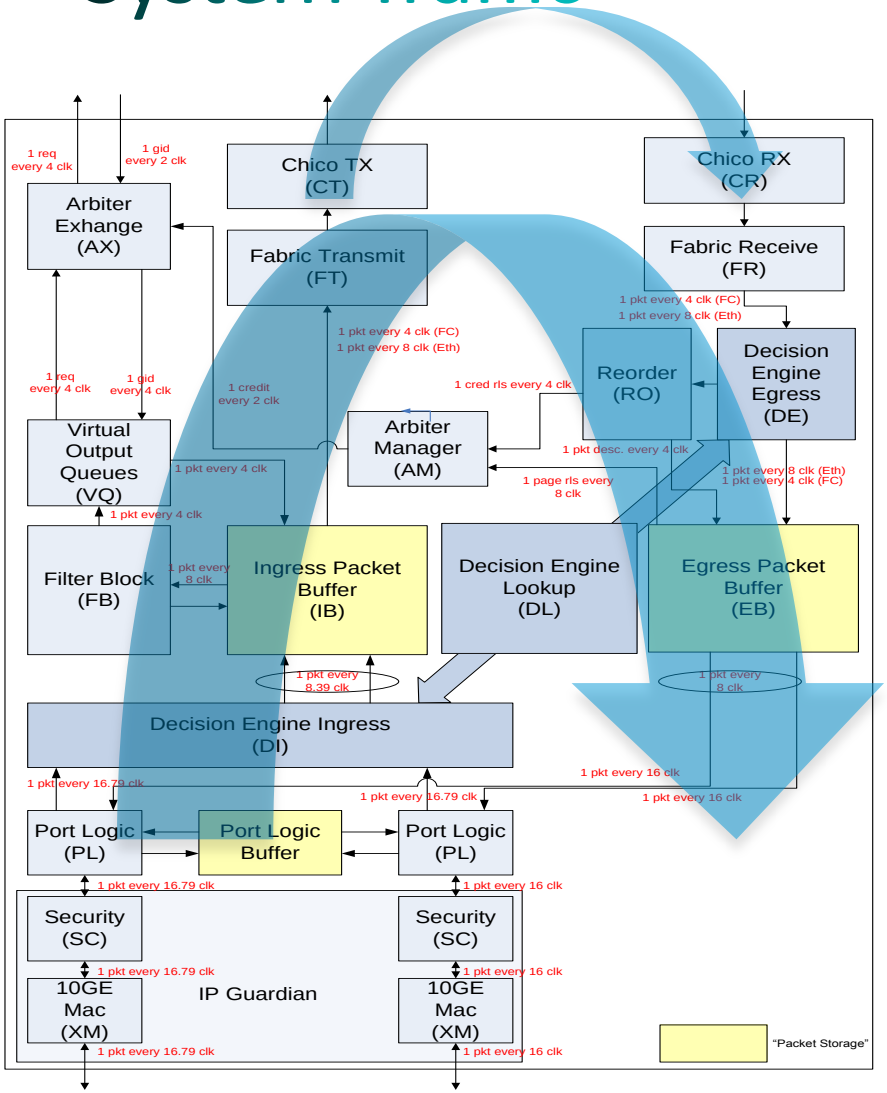
ASIC Top Fail Categories (MFG data)



Supplier Testing



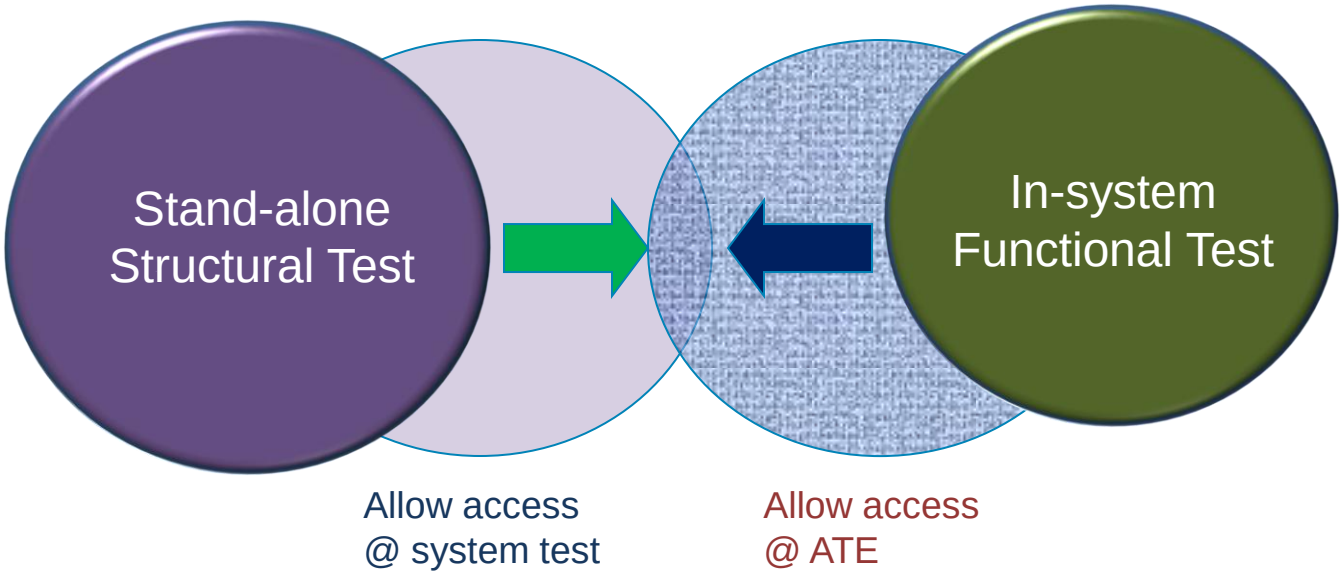
System Traffic



Potential Answers to Bridge the Gap

- Increase existing supplier DFT and test requirements
- Earlier engagement and partnership with suppliers on their bring-up, characterization and test
  - particularly for skew lots and correlation to system level performance
- Add functional testing at the ASIC supplier
- Analyze failure modes for un-modeled defects
- Brainstorm new and improved xBIST

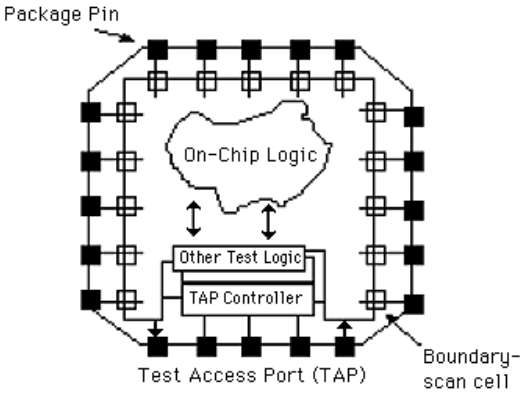
Bridging solution



- At board/system test
  - Enable functional-diag run standalone ASIC level test
  - Can detect marginal parts (e.g. BIST via JTAG)

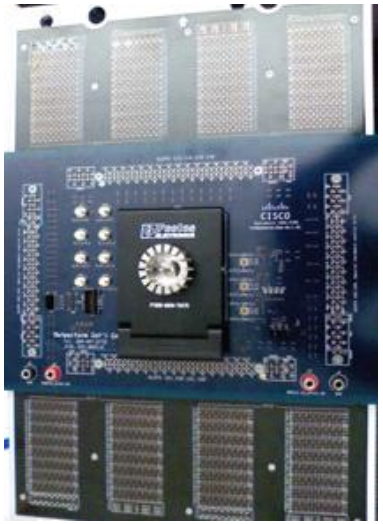
- At ATE test
  - Develop on chip functional test (functional IP)
  - Port the functional vector to ATE (access through JTAG or PCIe)

Enablers to the bridging solution

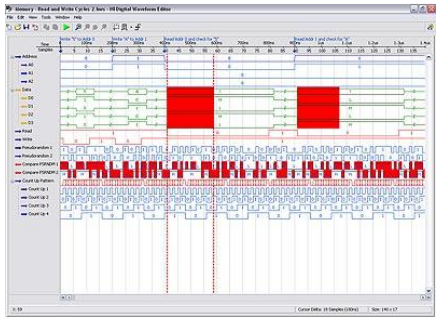


(1) On chip test access mechanism + DFT IPs

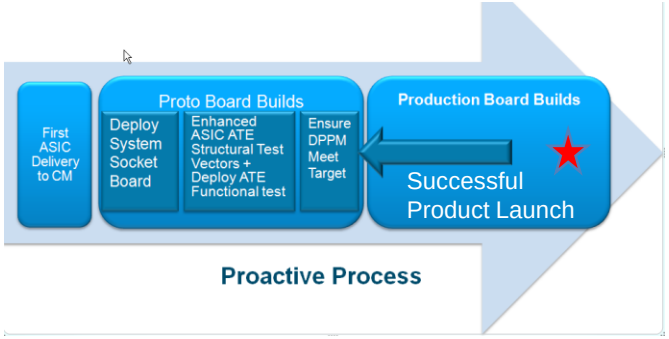
(2) Socket system



(3) ATE load board

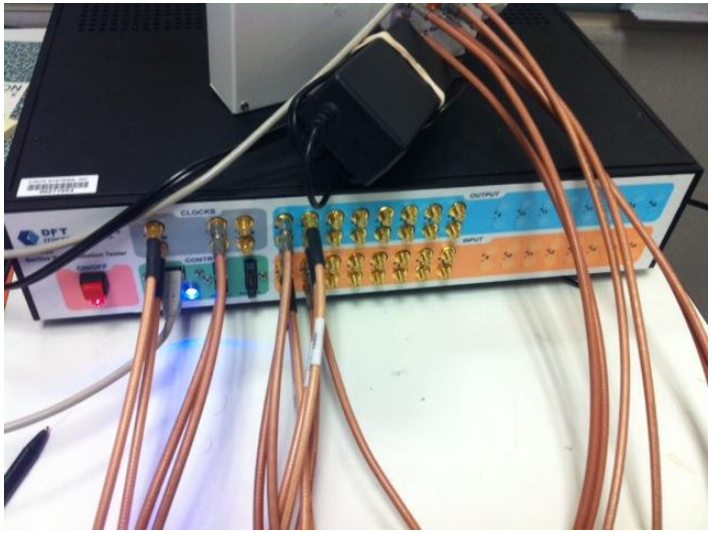


(4) Vector Conversion Tools

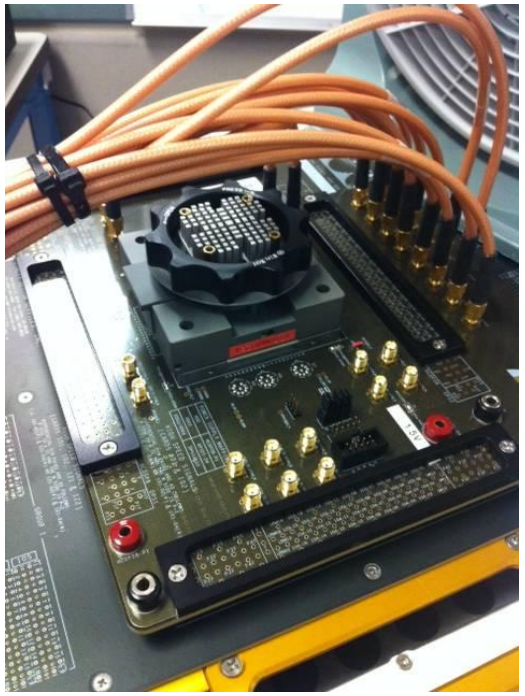


(5) Process Improvement

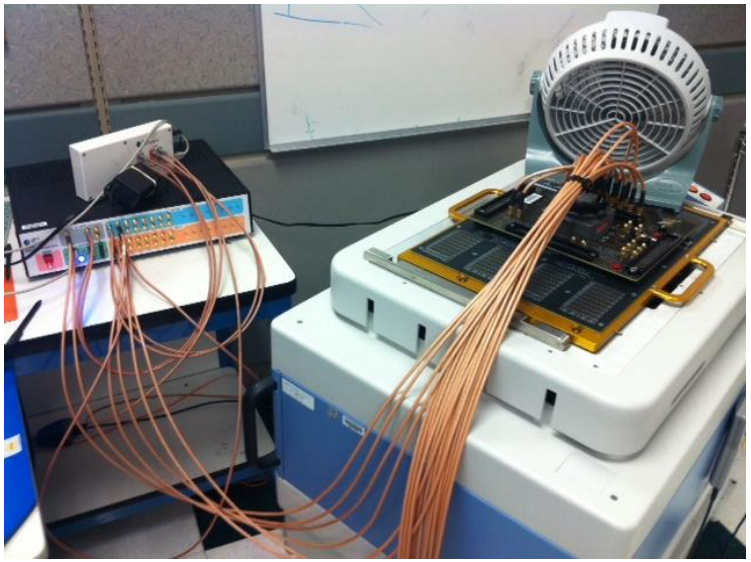
Enabling functional test @ATE



(a) DFT Micro's protocol aware system



(b) ATE test fixture with PCIe interface



Entire setup
using Verigy Pinscale

Closing the Gap

- Proactively porting Functional testing at suppliers
- Continued improvement on ASIC DFT and test coverage and correlation of supplier to system test
- Improved Memory modeling and testing
- Enhanced board diagnostic data capturing and analysis
- Innovative BIST techniques driven by continued learning and analysis on the gap

Ask of Engineering Community

- ASIC /SOC Requirements
  - Memory BISTs, Logic BIST, JTAG2CPU interface,
  - Functional MBIST (CPU based memory test)
  - Functional LBIST (CPU based logic test)
  - Programmable clock controllers
- Increased correlation of system to supplier test
- Enhanced board diagnostics
- Any new inputs?

Thank you.